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TRANSMITTAL LETTER AND AUTHORIZATION TO CHARGE DEPOSIT ACCOUNT

ASSISTANT COMMISSIONER FOR PATENTS
ALEXANDRIA, VA 22313

RE: Attorney Docket No.: OSEM-DB3
Application No.: 09/636,484
Filed: 08/10/00
Title: INTEGRATED TRANSISTOR DEVICES
Inventor: Braddock, David

SIR:

Attached hereto for filing are the following papers:

37 CFR 1.193 REPLY BRIEF (IN TRIPLICATE)

Our check in the amount of $00.00 is attached covering the required fees.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 50-2106. A duplicate copy of this sheet is enclosed.

31518
PATENT TRADEMARK OFFICE

7/14/04
Date

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Printed: July 26, 2004 (6:14pm)
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OLD DOCKET NO: DB3

NEW DOCKET NO: OSEM-DB3

IN RE APPLICATION OF: Braddock

Examiner: KANG

SERIAL NO: 09/636,484 CONF. NO: 6691

GROUP ART UNIT: 2811

FILED: 08/10/00

TITLE: INTEGRATED TRANSISTOR DEVICES

TO: ASSISTANT COMMISSIONER OF PATENTS

37 CFR 1.193 REPLY BRIEF

Sir: This is the applicant's reply brief in response to the examiner's answer mailed 5/28/204

I. Why the claims do not stand or fall together

Answer page 2 lines 21-23 the examiner asserts that claims 36 and 38 stand or fall together because appellants brief does not allege that the claims do not stand or fall together and are not separately argued. In reply, page 7 line 8 of the supplement appeal brief expressly states that the claims do not stand or fall together. Even if the panel sustains the rejection of claim 36, it may reverse the rejection of claim 38 on the basis that performance of the device disclosed in Passlack '718 patent is so poor that many such devices could not be used in an integrated circuit, and because claim 38 does not include the AlGaAs, InGaP, or InP alternatives present in claim 36. Moreover, the applicant admitted in the main brief that the InGaP alternative in claim 36 is inoperative and was claimed in error (and offered an amendment after final to correct that error which the examiner did not enter), so the panel may enter a rejection of claim 36 in applicable to claim 38. See the second Braddock declaration paragraph 3. Moreover, section IV below provides an additional reason why claim 36 is not suggested by the examiner's proposed combination.

II. Passlack '718 does not disclose the "gate insulator structure" Defined by Claims 36 and 38

At answer page 3 lines 21-22, the examiner again concludes that Passlack '718 discloses an (1) "enhancement mode Metal-Oxide compound Semiconductor Field Effect Transistor" (MOSFET) having (2) " a gate insulator structure.". In fact, Passlack '718 does not disclose either (1) or (2). Moreover, the examiner has not addressed in any way, either by impugning the inventor's credibility, expertise, or factual correctness of the inventor's assertions that Passlack '718 does not disclose a compound semiconductor MOSFET having (2), the "gate insulator structure" defined by both claims 36 and 38. See paragraphs 4 - 7 in the second declaration of David Braddock of record (filed April 29, 2003). These paragraphs assert that Ga2O3 is not insulating and that the Passlack '718 patent's Ga2O3 layer is therefore not "a gate insulator structure." That assertion is backed up by evidence of record, attachment 1 filed with the supplemental appeal brief originally filed April 29, 2003 and of record because that application was NOT under final when that appeal brief was filed. Attachment 1 (Preprint of Chapter 12,

Gallium Oxide on Gallium Arsenide: Atomic Structure, Materials, and Devices, listing Passlack (first inventor of the Passlack '718 patent as the first named author) page numbered 347, second paragraph lists measured resistivity of only 400 to 700 Ohm-cm, and paragraph 3 estimates the maximum resistivity of Ga2O3 at less than 10,000 Ohm-cm. In attachment 1, page numbered 347, second paragraph, Passlack goes on to surmise that Ga2O3's observed "strong electrical conductivity only requires defect densities of 10[18] cm[-3] within the oxide bandgap...."

Moreover, Attachment 1 would indicate to one skilled in the art that Ga2O3 was an intrinsic n-type semiconductor, not an intrinsic insulator, as stated in paragraph 4 of the second 37 CFR 1.132 declaration of David Braddock.

The support for that conclusion are the following passages from attachment 1, and Dr. Braddock's explanation of what they mean to one skilled in the art. At page 347, paragraph 2, in attachment 1, Passlack indicates that Ga2O3 has an estimated conductivity of ten to the eighteenth per cubic centimeter, independent of polarity (see "Large leakage currents ... independent of polarity."; paragraph 2 lines 1-2). Dr. Braddock indicates that the polarity independence means inter alia that the Ga2O3 forms no rectifying junction with the underlying semiconductor.

Attachment 1 figure 17 page 347 indicates the use of n-type GaAs in a Ga2O3-GaAs structure. See figure caption to figure 17 (showing "Ga2O3/n-GaAs"). Dr. Braddock indicates that this means that Attachment 1's Ga2O3 was in fact an n-type conductor because Attachment 1 indicates that there is no polarity dependence to the I-V characteristics as would occur if the Ga2O3 were p-type.

Attachment 1, page 347, paragraph 2, states that "The lack of response to active oxygen exposure suggests that the defects responsible for conduction are not related to oxygen vacancies or the defect nature of the amorphous network is complex and defects cannot be removed by exposure to active oxygen under the above discussion conditions." However, attachment 1 page 347, paragraph 2 also states that post-deposition annealing and oxygenation only "marginally improved" the "bulk properties" of Ga2O3, and Dr. Braddock indicates that oxygenation and post deposition annealing are techniques used to remove defects. Since oxygenation and post deposition annealing are did not result in insulating properties, the alternative and more logical conclusion is that Ga2O3 is not an insulator. Thus, Passlack's evidence suggests that the Ga2O3

is in fact an intrinsic n-type semiconductor, and that would have been obvious to one of ordinary skill in the art.

Attachment 1, page 348, paragraph 1 states that "quasi static C-V curves cannot be acquired due to high leakage current. Dot size of 500, 250, and 50 um diameter are measured." What this means is that the Ga2O3-GaAs structure upon which this data is based is one where the Ga2O3 has the residual n-type conductivity of ~10 E 18 cm-3 as noted on page 347 paragraph 2. This conductivity is so high that quasi static C-V data could not be obtained. However, a quasi-static C-V measurement is a standard mechanism used to characterize MOS structures, and Dr. Braddock indicates that the ability to make a quasi-static C-V measurement is used by the silicon semiconductor industry to verify whether an MOS structure in fact exists. Thus, Dr. Braddock asserts that the fact that Attachment 1 admits that quasi static C-V data could not be obtained indicates to one skilled in the art that the Ga2O3 in the device under test was not an insulator structure suitable for a MOSFET.

Moreover, at answer page 6 lines 5-12, the examiner admits that he equated Passlack's disclosed oxide with a gate insulator "because the terms, gate oxide and gate insulator, are often used interchangeably in the art." That is, the examiner admits he did not recognize the functional distinction between oxide and insulator. Passlack '718 does not refer to an insulator. Not all oxides are insulators. Ga2O3 is such a non-insulator oxide. Indium Tin oxides are others. Accordingly, you can stop reading here, and reverse the rejections.

III. Additional Evidence, and Why You Should Consider it, 37 CFR 1.195 NotWithStanding, that Shows that Passlack '718 does not Disclose a Gate Insulator Structure or an Enhancement Mode MOSFET

In response to the examiner's assertion that Passlack '718 discloses a MOSFET, you should consider the Johnson declaration, attachment 7, and the Accuratus data, attachment 8, to the amendment filed 7/21/2004, 37 CFR 1.195 notwithstanding. 37 CFR 1.195 notwithstanding at least because, in my opinion, the procedural state of this application is ambiguous. As it stands as of 7/19/2004, there are outstanding petitions regarding the restriction and impropriety of the examiner's procedural actions in not entering an appeal brief and subsequently filed amendments

and evidence. See for example petition filed June 14, 2004 first and second full paragraphs. It is my belief that those petitions should eventually be granted and all of the evidence and additional claims will at that point be entered and considered. However, if you agree that the papers should be entered (and not to do so would be to contradict your binding precedent in Ex parte Lemoine, 46 USPQ2d 1420, ___ (PTOBPAI 1994)(precedential decision of an expanded panel including APJ Schafer, APJ Meister, SAPJ McKelvey, and CAPJ Stoner), you should consider the Johnson declaration and the related evidence not yet of officially of record - or you should await the Director's decision on the petitions. The issue of whether you hear that evidence raises a question of jurisdiction of the Board similar to Lemoine (whether evidence properly filed but improperly not admitted at time an appeal is heard can or must be considered by the panel hearing the appeal; whether the Board has jurisdiction to determine the merits of a pending petition affecting Board jurisdiction over an appeal) which you should consider.

The Johnson declaration shows that the Dr. Braddock's statements that Passlack '718 does not disclose an gate insulator structure is correct, explains why Passlack '718 does not in fact disclose a MOSFET, and explains why some of the examiner's factual contrary assertions are wrong. Dr. Johnson explains that the Passlack '718 patent does not disclose to one of ordinary skill in the art a MOSFET because the Passlack '718' s Ga2O3 layer as disclosed in the '718 patent does not provide the function of a gate insulator of a MOSFET. As Dr. Johnson points out, what Passlack '718 purports to discloses (without reference to subsequent evidence showing that Ga2O3 is in fact not an insulator) to one of ordinary skill in the art is a MESFET, and not a MOSFET. Thus, the Passlack '718 patent does not in fact disclose either (1) "enhancement mode Metal-Oxide compound Semiconductor Field Effect Transistor" or (2) " a gate insulator structure.". If you agree, you can stop reading at this point and reverse the rejections of claims 36 and 38.

Accuratus, attachment 8 shows on its page 2 that SiO2, which is an insulator, has a volume resistivity of greater than ten to the tenth Ohm-cm. Compare that to the volume resistivity that Passlack reports for Ga2O3 in his book chapter 12 as published, attachment 5 to the amendment filed July 21, 2004 (which is the published version of the of record pre-publication version of this book chapter 12) page 341-2 of 400 Ohm-cm to ten thousand Ohm-cm. The difference of at least

6 orders of magnitude in resistivity between SiO2 and Ga2O3 is another indication that Ga2O3 is not an insulator, and therefore Passlack '718 does not disclose a gate insulator structure of a MOSFET, as is defined by claims 36 and 38. Accordingly, the additional evidence shows that Passlack '718 does not disclose the gate insulator structure or an enhancement mode MOSFET as defined by claims 36 and 38.

IV. The Examiner's Propose Combination is Not Subject Matter Defined by Claim 36

At answer page 4 lines 7-12 and page 7 line 9 the examiner relies upon column 16 lines 5-9 in Kikkawa, arguing that Kikkawa suggests that Passlack's GaAs substrate can be replaced with an InP substrate. Assuming arguendo that the examiner's proposed combination is legally obvious, it does not result in the claimed subject matter (claim 36 or claim 38). This is because the claimed subject matter (claims 36 and 38) define an interface with the gate insulator structure/semiconductor interface in which the semiconductor is not GaAs, and the examiner's proposed combination requires a gate insulator/GaAs interface.

Passlack '718 teaches a GaAs/Ga2O3 interface. In fact, the existence of an atomically abrupt low defect density interface is the primary technical teaching of Passlack '718. Column 3 lines 28-37, particularly lines 35-37, and column 4 lines 62 to column 5 line5, and claim 8. Thus, the disclosure of the GaAs top layer in Passlack '718 is apparently essential to Passlack's invention. The modification proposed by the examiner does not suggest removing the GaAs top layer. The examiner's proposed combination replaces the Passlack '718 structure's GaAs substrate with an InP substrate arguing that Kikkawa provides motivation for that modification.

Claims 36 recites "a compound semiconductor wafer structure having an upper surface; and "a gate insulator structure positioned on upper surface of said compound semiconductor wafer structure." Figures 1 and 2 (steps 102-104) the description thereof in the specification at page 16 lines 13-16 indicate that "positioned on" means an interface. Similarly, the recitation of "a gate electrode positions on said gate insulator structure" wherein the specification shows that "positioned on" means an interface.

That construction also follows from the connection in claim 36 of the recitation that the AlGaAs, InGaAs, InP, or InGaP layer of the semiconductor wafer structure "being positioned on

said upper surface" of the semiconductor wafer structure, even though the claimed AlGaAs, InGaAs, InP, or InGaP layer is defined in claim 36 as part of the semiconductor wafer structure. In other words, the language of claim 36 is strained to show that the AlGaAs, InGaAs, InP, or InGaP layer contacts the gate insulator structure. Moreover, by definition of a MOSFET (claim 36's preamble defines a MOSFET), the gate is on the semiconductor in the sense that it is deposited on/in contact with the semiconductor. Hence, the broadest reasonable construction of claim 36 is a structure in which the AlGaAs, InGaAs, InP, or InGaP layer is in contact with the "gate insulator structure." The examiner's proposed combination has Passlack '718 's AlGasAs spacer layer 23, then the GaAs top spacer layer 15, and then a Ga2O3 layer. The examiner's proposed combination does not have an AlGaAs layer interfacing to a Ga2O3 layer. Therefore, the proposed combination is not subject matter defined by claim 36, even if the proposed combination is legally obvious and even if Ga2O3 is deemed a "gate insulator structure." For this additional reason, the rejection of claim 36 should be reversed.

V. Response to Miscellaneous Assertions in the Examiner's Answer

At answer page 6 lines 10-12, the examiner misconstrues the specification page 7 paragraph 2. In reply, in fact, the specification consistently refers to a gate insulator structure as a structure including more than one layer.

At answer page 7 line 16, the examiner asserts that page 4 third paragraph is inconsistent with lack of motivation to modify Passlack in view of Kikkawa. In reply, presumably the examiner is referring to the originally filed specification and the background discussion of why GaAs and InP based complementary technologies have limited commercial success. If so, that reference is irrelevant to the obviousness issue.

VI. Clarifications of Statements in Dr. Braddock's Declarations Directed to the Combination Rejection, Why the Prior Art Does Not Suggest the Proposed Combination, and Dr. Braddock's retraction of Statements in Paragraph 8e-8h in his Second Declaration

In reply, upon careful review, the applicant notes that Passlack '718 discloses InGaAs for the channel layer, but disclose AlGaAs and InGaP as the wider gap space layer. See for example Passlack '718 claim 13. Much of Dr. Braddock's factual assertions were directed to the upper layer, which is the wider band gap spacer layer. Upon review, the applicant believes that Kikkawa suggests using an In containing channel layer as a dry etch stop, and that Kikkawa's statements respecting alternatives at column 16 lines 5-10 relate to Indium containing alternatives to the InGaAs channel layer.

The applicant admits that modifying Passlack '718 to include an InP substrate and the InGaAs channel layer common to both Kikkawa and Passlack '718 would be feasible. However, including as the upper spacer layer AlGaAs or InGaP would introduce strain and certainly defects into the combined structure. Therefore, while it might be feasible to fabricate a InP/InGaAs/AlGaAs or InP/InGaAs/InGaP structure similar to the GaAs substrate structure disclosed in Passlack '718, Passlack '718's teaching of the desirability of a low defect density GaAs surface upon which to deposit stoichiometric Ga2O3 having a lower interface defect density teaches away from such structures. Accordingly, given Passlack '718's teachings and Kikkawa's teachings, it would not be legally obvious to make these combinations. Moreover, Passlack teaches the desirability of the upper wider band gap spacer layer, and therefore, the art relied upon in the rejections provides no motivation to not include that upper wider band gap spacer layer. Accordingly, there is no legal motivation. For this additional reason, the rejections of claims 36 and 38 should be reversed.

Given this explanation, please note that Dr. Braddock wishes to clarify certain statements in his declarations that relate to this argument.

In the first and second declarations of Dr. Braddock, numbered paragraph 3 in both declarations, the statement "The applied Passlack patent teaches using only AlGaAs or InGaP lattice matched" should be clarified to read "The applied Passlack patent teaches using only AlGaAs or InGaP wider gap spacer layers lattice matched...."

In the second declaration, Dr. Braddock now believes that numbered paragraph 8e is incorrect. Dr. Braddock made the statements in this paragraph based upon interpreting column 16 lines 5-10 in Kikkawa as requiring antimonides in alternative embodiments including an InP

substrate. However, upon careful review, as noted above, it appears that Kikkawa is suggesting Indium containing alternatives to the InGaAs etch stop layer of the Figure 9 embodiment, and therefore, Indium containing compounds in connection with an InP substrate. Dr. Braddock knows that at least some III-V Indium containing compounds can lattice match to an InP substrate, including for example InGaAs.

Given the foregoing reinterpretation of Kikkawa, Dr. Braddock believes that paragraph 8e-8h in his second declaration are either incorrect or not relevant. Dr. Braddock withdraws paragraphs 8e-8h in his second declaration.

Respectfully Submitted,

7/26/04

Date

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Printed: July 26, 2004 (5:01pm)
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